

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. For all tests, $V_1 = VS_1$, $V_2 = VS_2$, $V_3 = VS_3$. Unless otherwise noted, $V_1 = V_2 = V_3 = V_{OUT} = 12\text{V}$, $HYS = GND$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Start-Up							
V_1 - V_3 , V_{OUT}	V_1 to V_3 , V_{OUT} Operating Supply Range		●	2.5	36	V	
$I_{V_1-V_3, V_{OUT}(EN)}$	Total Supply Current with Channels Enabled	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = 4\text{V}$, (Notes 3, 4)	●	28	78	μA	
$I_{V_1-V_3(EN)}$	Total Supply Current with Channels Disabled	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = EN = 0\text{V}$, (Notes 3, 4)	●	26	93	μA	
$I_{V_1-V_3(SHDN)}$	Total Supply Current When Shutdown	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = \overline{\text{SHDN}} = 0\text{V}$, (Notes 3, 4)	●	15.4	84	μA	
$I_{V_{OUT}}$	V_{OUT} Supply Current	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = 4\text{V}$	●	14	30	μA	
$I_{PRIORITY}$	Current from Highest V_1 to V_3 Priority Input Source (V_1)	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = 4\text{V}$ $V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = EN = 0\text{V}$	●	2.6	6	μA	
$I_{HIGHEST}$	Current from Highest V_1 to V_3 Voltage Input Source	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = 4\text{V}$, (Note 3, 4)	●	11	72	μA	
		$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = EN = 0\text{V}$, $\overline{\text{SHDN}} = 0\text{V}$, (Note 3, 4)	●	15	80	μA	
I_{LOWER}	Current from V_1 to V_3 Input Voltage Sources Lower than V_{OUT}	$V_1 = 5\text{V}$, $V_2 = 12\text{V}$, $V_3 = 2.5\text{V}$, $V_{OUT} = 4\text{V}$ Not Highest Valid Priority		-5	0.2	1	μA
Gate Control							
ΔV_G	Open ($VS - VG$) Clamp Voltage	$V_{OUT} = 11\text{V}$, G_1 to $G_3 = \text{Open}$	●	5.2	6.2	6.7	V
$\Delta V_{G(SOURCE)}$	Sourcing ($VS - VG$) Clamp Voltage	$V_{OUT} = 11\text{V}$, $I = -10\mu\text{A}$	●	5.8	6.6	7	V
$\Delta V_{G(SINK)}$	Sinking ($VS - VG$) Clamp Voltage	$V_{OUT} = 11\text{V}$, $I = 10\mu\text{A}$	●	4.5	5.2	6	V
$\Delta V_{G(OFF)}$	G_1 to G_3 Off ($VS - VG$) Threshold	$V_1 = V_2 = V_3 = 2.8\text{V}$, $V_{OUT} = 2.6\text{V}$, G_1 to G_3 Rising Edge	●	0.12	0.35	0.6	V
$\Delta V_{G(SLEW, ON)}$	G_1 to G_3 Pull-Down Slew Rate	$V_{OUT} = 11\text{V}$, $C_{GATE} = 10\text{nF}$ (Note 5)	●	4	9	20	$\text{V}/\mu\text{s}$
$\Delta V_{G(SLEW, OFF)}$	G_1 to G_3 Pull-Up Slew Rate	$V_{OUT} = 11\text{V}$, $C_{GATE} = 10\text{nF}$ (Note 6)	●	5.5	10	22	$\text{V}/\mu\text{s}$
$I_{G(DN)}$	G_1 to G_3 Low Pull-Down Current	$V_{OUT} = 2.6\text{V}$, V_1 to $V_3 = 2.8\text{V}$, (G_1 to G_3) = $\Delta V_G + 300\text{mV}$		0.8	2	7	μA
$R_{G(OFF)}$	G_1 to G_3 OFF Resistance	$V_{OUT} = 4\text{V}$, V_1 to $V_3 = 5\text{V}$, $I_G = -10\text{mA}$	●	9	22	40	Ω
V_{REV}	Reverse Voltage Threshold	Measure (V_1 to V_3) - V_{OUT} , V_{OUT} Falling	●	30	120	200	mV
$t_{G(SWITCHOVER)}$	Pin Break-Before-Make Time	$V_{OUT} = 11\text{V}$, $C_{GATE} = 10\text{nF}$, (Note 7)	●	0.7	2	3.2	μs
$t_{pG(SHDN)}$	G_1 to G_3 Turn-Off Delay From $\overline{\text{SHDN}}$	$V_{OUT} = 11\text{V}$, Falling Edge $\overline{\text{SHDN}}$ to (G_1 to G_3) = (VS_1 to VS_3) - 3V, $C_{GATE} = 10\text{nF}$	●	20	50	100	μs
$t_{pG(EN, OFF)}$	G_1 to G_3 Turn-Off Delay From EN	$V_{OUT} = 11\text{V}$, Falling EN Edge to (G_1 to G_3) = (VS_1 to VS_3) - 3V, $C_{GATE} = 10\text{nF}$	●	0.3	0.7	1.4	μs
$t_{pG(EN, ON)}$	G_1 to G_3 Turn-On Delay From EN	$V_{OUT} = 11\text{V}$, Rising EN Edge to (G_1 to G_3) = (VS_1 to VS_3) - 3V, $C_{GATE} = 10\text{nF}$	●	0.9	1.3	2	μs

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS			
Input/Output Pins									
$V_{\text{VALID(OL)}}$	VALID1 to VALID3 Output Low Voltage	$I = 1\text{mA}$, (V_1 to V_3) = 2.5V, $V_{\text{OUT}} = 0\text{V}$	●	0.25	0.55	V			
$t_{\text{pVALID(OFF)}}$	VALID1 to VALID3 Delay OFF From OV/UV Fault		●	5	8	13	μs		
$V_{\text{CAS(OH)}}$	CAS Output High Voltage	$I = -1\mu\text{A}$	●	1.4	2.2	3	V		
$V_{\text{CAS(OL)}}$	CAS Output Low Voltage	$I = 1\text{mA}$	●	0.08	0.2	0.4	V		
I_{CAS}	CAS Pull-Up Current	$\text{SHDN} = 0\text{V}$, $\text{CAS} = 1\text{V}$	●	-6	-30	-20	-50	-40	μA
$t_{\text{pCAS(EN)}}$	CAS Delay from $V_{\text{G(OFF)}}$	$V_{\text{OUT}} = 11\text{V}$	●	0.4	0.9	0.7	1.4	1.3	μs
$V_{\text{EN(THR)}}$	EN Threshold Voltage	EN Rising	●	0.6	1.1	1.4	V		
$V_{\text{SHDN(THR)}}$	SHDN Threshold Voltage	SHDN Rising	●	0.4	0.8	1.2	V		
$V_{\text{SHDN_EN(HYS)}}$	SHDN, EN Threshold Hysteresis			130	100		mV		
$I_{\text{SHDN_EN}}$	SHDN, EN Pull-Up Current	$\text{SHDN} = \text{EN} = 0\text{V}$	●	-0.5	-3	-2	-5	μA	
I_{LEAK}	SHDN, EN, VALID1 to VALID3, CAS Leakage Current	$\text{SHDN} = \text{EN} = (\text{VALID1 to VALID3}) = 36\text{V}$, $\text{CAS} = 5.5\text{V}$	●			± 1	μA		
OV, UV Protection Circuitry									
$V_{\text{OV_UV(THR)}}$	OV1 to OV3, UV1 to UV3 Comparator Threshold	$V_{\text{OUT}} = 11\text{V}$, OV1 to OV3 Rising, UV1 to UV3 Falling	●	0.985	1	1.015	V		
$V_{\text{OV_UV(HYS)}}$	OV1 to OV3, UV1 to UV3 Comparator Hysteresis	$V_{\text{OUT}} = 11\text{V}$	●	15	30	45	mV		
$I_{\text{UV_OV(LEAK)}}$	OV1 to OV3, UV1 to UV3 Leakage Current	OV1 to OV3 = 1.015V, UV1 to UV3 = 0.985V	●			± 20	nA		
$I_{\text{OV_UV(MIN)}}$	Minimum External Hysteresis Current	$I_{\text{HYS}} = -400\text{nA}$	●	35	55	50	75	nA	
$I_{\text{OV_UV(MAX)}}$	Maximum External Hysteresis Current	$I_{\text{HYS}} = -4\mu\text{A}$	●	420	520	620	nA		
V_{HYS}	HYS Voltage	$I_{\text{HYS}} = -4\mu\text{A}$	●	470	495	520	mV		
t_{VALID}	V1 to V3 Validation Time			100	256	412	ms		

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Each V1 to V3 supply current specification includes current into the corresponding VS1 to VS3 for the channel(s) being tested.

Note 4: Specification represents the total diode-ORed current of V1 to V3 input supplies, selecting the highest voltage as the input source. If two input supplies are similar in voltage and higher than the remaining input supply voltage, the current is split evenly between the two higher voltage supplies. Current is split evenly if all supplies are equal.

Note 5: Falling edge of G1 to G3 measured from 11V to 8V.

Note 6: Rising edge of G1 to G3 measured from 7V to 11V.

Note 7: UV1 driven below $V_{\text{OV,UV(THR)}}$. Time is measured from respective rising edge G1 to G3 crossing (VS1 to VS3) – 3V to next valid priority falling edge G1 to G3 crossing (VS1 to VS3) – 3V.